IN THE CLAIMS:

1. (original) A method of forming a layer of interconnect in an integrated circuit comprising the steps of:

depositing a first layer of interlayer dielectric on a lower layer of said integrated circuit above a set of lower alignment marks;

depositing a first hardmask layer of TaN on said first layer of ILD, said first layer being substantially transparent in a relevant wavelength range;

forming an upper set of alignment marks;

patterning said ILD through said hardmask layer to form a set of apertures in said ILD; and

forming a conductive interconnect in said set of apertures.

2. (original) A method according to claim 1, in which said hardmask layer is deposited by sputter deposition of Ta in an ambient containing N_2 and a carrier gas such that $(N_2 flow)/(N_2 + carrier\ flow) > 0.5$.

3. (original) A method according to claim 1, in which said hardmask layer is deposited by chemical vapor deposition by reacting a precursor gas containing Ta in an ambient containing N_2.

4. (original) A method according to claim 2, in which said hardmask layer is substantially transparent in said relevant wavelength range.

5. (original) A method according to claim 3, in which said hardmask layer is substantially transparent in said relevant wavelength range.

6. (original) A method according to claim 2, in which said hardmask layer has a resistivity greater than about 400 Ohm-cm.

7. (original) A method according to claim 3, in which said hardmask layer has a resistivity greater than about 400 Ohm-cm.

8. (original) A method according to claim 2, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

9. (original) A method according to claim 3, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

10. (original) A method according to claim 2, in which said hardmask layer has a composition of less than 50% Ta.

11. (original) A method according to claim 3, in which said hardmask layer has a composition of less than 50% Ta.

12. (withdrawn) An integrated circuit comprising:

a semiconductor substrate containing a set of devices;

a first layer of interlayer dielectric (ILD) on a lower layer of said integrated circuit above a set of lower alignment marks;

a first hardmask layer of TaN on said first layer of ILD, said first hardmask layer and said first ILD being substantially transparent in a relevant wavelength range;

an upper set of alignment marks;

a set of apertures in said ILD; and

a conductive interconnect in said set of apertures.

13. (withdrawn) An integrated circuit according to claim 12, in which said hardmask layer is deposited by sputter deposition of Ta in an ambient containing N_2 and a carrier gas such that (N_2flow)/(N_2 + carrier flow) > 0.5.

14. (withdrawn) An integrated circuit according to claim 12, in which said hardmask layer is deposited by chemical vapor deposition by reacting a precursor gas containing Ta in an ambient containing N_2.

15. (withdrawn) An integrated circuit according to claim 13, in which said hardmask layer is substantially transparent in said relevant wavelength range.

16. (withdrawn) An integrated circuit according to claim 14, in which said hardmask layer is substantially transparent in said relevant wavelength range.

17. (withdrawn) An integrated circuit according to claim 13, in which said hardmask layer has a resistivity greater than about 400 Ohm-cm.

18. (withdrawn) An integrated circuit according to claim 14, in which said hardmask layer has a resistivity greater than about 400 Ohm-cm.

19. (withdrawn) An integrated circuit according to claim 13, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

20. (withdrawn) An integrated circuit according to claim 14, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

21. (withdrawn) An integrated circuit according to claim 13, in which said hardmask layer has a composition of less than 50% Ta.

22. (withdrawn) An integrated circuit according to claim 14, in which said hardmask layer has a composition of less than 50% Ta.